ABSTRACT OF THE DISCLOSURE

DRAM cell arrangement with vertical MOS transistors, and method for its fabrication. Channel regions arranged along one of the columns of a memory cell matrix are parts of a rib which is surrounded by a gate dielectric layer. Gate electrodes of the MOS transistors belonging to one row are parts of a strip-like word line, so that at each crossing point of the memory cell matrix there is a vertical dual-gate MOS transistor with gate electrodes of the associated word line formed in the trenches on both sides of the associated rib.